Amendments to the CLAIMS:

Without prejudice, this listing of the claims replaces all prior versions and listings of the claims in the present application:

LISTING OF CLAIMS:

1. (Currently Amended) A multiplexing and transmission apparatus which receives low-speed frame signals from a plurality of channels in parallel and outputs a high-speed serial signal, said multiplexing and transmission apparatus comprising:

a control pulses generating circuit which generates control pulses each of which corresponds to one of said channels, wherein ~~phases~~ of said control pulses ~~are~~ have different timing for each channel;

channel-frame generating circuits, connected to said control pulses generating circuit, each of which receives said low-speed frame signal and outputs said low-speed frame signal in synchronization with said control pulse so that an output timing of said low-speed frame signal is shifted with respect to an output timing of other low-speed frame signals so that a receiving side apparatus can recognize a channel number of said low-speed frame signal; and

a multiplexing circuit, connected to said channel-frame generating circuits, which multiplexes said low-speed frame signals into said high-speed serial signal and outputs said high-speed serial signal.

2. (Currently Amended) A multiplexing and transmission apparatus which receives a high-speed serial signal, demultiplexes said high-speed serial signal into low-speed frame signals and outputs said low-speed frame signals to a plurality of channels in parallel, said multiplexing and transmission apparatus comprising:

a demultiplexer which demultiplexes said high-speed serial signal into said low-speed frame signals;

channel-frame synchronization circuits, connected to said demultiplexer, each of which receives said low-speed frame signal, generates a frame pulse corresponding to said low-speed frame signal, and outputs said low-speed frame signal;

a switching circuit, connected to said channel-frame synchronization circuits, which receives said low-speed frame signals and sends each of said low-speed frame signals to an appropriate port of said channel; and

a switch controller circuit which controls said switching circuit according to said frame pulses output from said channel-frame synchronization circuits,

wherein each of said channel-frame synchronization circuits establishes a frame synchronization on a channel-by-channel basis and outputs said frame pulse which indicates a head position of said low-speed frame signal, and

said switch controller circuit identifies channel numbers of said low-speed frame signals according to a time difference for receiving said frame pulses, and controls said switching circuit.

3. (Currently Amended) A multiplexing and transmission apparatus which receives send low-speed frame signals from a plurality of send channels in parallel, outputs a send high-speed serial signal, receives a receive high-speed serial signal, demultiplexes said receive high-speed serial signal into receive low-speed frame signals and outputs said receive low-speed frame signals to a plurality of receive channels in parallel, said multiplexing and transmission apparatus comprising:

a control pulses generating circuit which generates control pulses each of which corresponds to one of said send channels; wherein phases of said control pulses are different for each send channel;

channel-frame generating circuits, connected to said control pulses generating circuit, each of which receives said send low-speed frame signal, and outputs said send low-speed frame signal in synchronization with said control pulse;

a multiplexing circuit, connected to said channel-frame generating circuits, which multiplexes said send low-speed frame signals into said send high-speed serial signal and outputs said send high-speed serial signal;

a demultiplexer which demultiplexes said receive high-speed serial signal into said receive low-speed frame signals;

channel-frame synchronization circuits, connected to said demultiplexer, each of which receives said receive low-speed frame signal, generates a frame pulse corresponding to said receive low-speed frame signal, and outputs said receive low-speed frame signal;

a switching circuit, connected to said channel-frame synchronization circuits, which receives said receive low-speed frame signals and sends each of said receive low-speed frame signals to an appropriate port of said receive channel; and

a switch controller circuit which controls said switching circuit according to said frame pulses output from said channel-frame synchronization circuits,

wherein each of said channel-frame synchronization circuits establishes a frame synchronization on a channel-by-channel basis and outputs said frame pulse which indicates a head position of said low-speed frame signal, and

said switch controller circuit identifies channel numbers of said low-speed frame signals according to a time difference for receiving said frame pulses, and controls said switching circuit.

4. (Original) The multiplexing and transmission apparatus as claimed in claim 1, said multiplexing and transmission apparatus further comprising:

synchronization pattern inserting circuits each of which inserts a frame synchronization pattern into said low-speed frame signal.

5. (Currently Amended) The multiplexing and transmission apparatus as claimed in claim 1, wherein a time duration on which said control pulses are generated for every channel is smaller than a time duration of a channel-frame format.

6. (Currently Amended) ~~The multiplexing and transmission apparatus as claimed in claim 5,~~ A multiplexing and transmission apparatus which receives low-speed frame signals from a plurality of channels in parallel and outputs a high-speed serial signal, said multiplexing and transmission apparatus comprising:

a control pulses generating circuit which generates control pulses each of which corresponds to one of said channels, wherein phases of said control pulses are different for each channel;

channel-frame generating circuits, connected to said control pulses generating circuit, each of which receives said low-speed frame signal and outputs said low-speed frame signal in synchronization with said control pulse; and

a multiplexing circuit, connected to said channel-frame generating circuits, which multiplexes said low-speed frame signals into said high-speed serial signal and outputs said high-speed serial signal;

wherein time duration on which said control pulses are generated for every channel is smaller than time duration of channel-frame format, and

wherein said control pulses generating circuit ~~comprising~~ includes:

a control clock generator;

a DC voltage generator;

a selector which outputs said control pulses sequentially for each channel according to control clock supplied from said control clock generator, said control pulses generated according to signals supplied from said DC voltage generator.

7. (Canceled).

8. (Currently Amended) The multiplexing and transmission apparatus as claimed in claim [[7]] 2, said switch controller circuit comprising:

a shift register which receives said frame pulses in parallel and shifts each of said frame pulses;

exclusive-OR circuits each of which is connected to said shift register and provided for each frame pulse;

demultiplexers each of which is connected to said exclusive-OR circuit and outputs a pattern indicating time position of said frame pulse;

a reset pulse generating circuit which initializes said demultiplexers according to receiving state of said frame pulse.

9. (Original) A computer readable medium storing program code for causing a computer to control a switching circuit in an multiplexing and transmission apparatus which receives a high-speed serial signal and demultiplexes said high-speed serial signal into low-speed frame signals, wherein said switching circuit assigns each of said low-speed frame signals to an appropriate port of a channel, said computer readable medium comprising:

program code means for receiving and storing frame pulses indicating head positions of said low-speed frame signals;

program code means for checking whether said frame pulses for every channel are stored;

program code means for reading said frame pulses and identifying receiving order of said low-speed frame signals; and

program code means for controlling said switching circuit on the basis of said receiving order so that said switching circuit assigns each of said low-speed frame signals to an appropriate port of a channel.

10. (Currently Amended) A multiplexing and transmission method used in an apparatus which receives low-speed frame signals from a plurality of channels in parallel and outputs a high-speed serial signal, said multiplexing and transmission method comprising the steps of:

generating control pulses each of which corresponds to one of said channels, wherein ~~phases~~ of said control pulses ~~are~~ have different timing for each channel;

receiving said low-speed frame signal and outputting said low-speed frame signal in synchronization with said control pulse for each of said low-speed frame signals so that an output timing of said low-speed frame signal is shifted with respect to an output timing of other low-speed frame signals so that a receiving side apparatus can recognize a channel number of said low-speed frame signal; and

multiplexing said low-speed frame signals into said high-speed serial signal and outputting said high-speed serial signal.

11. (Currently Amended) A multiplexing and transmission method used in an apparatus which receives a high-speed serial signal, demultiplexes said high-speed serial signal into low-speed frame signals and outputs said low-speed frame signals to a plurality of channels in parallel, said multiplexing and transmission method comprising the steps of:

demultiplexing said high-speed serial signal into said low-speed frame signals;

generating, for each of said low-speed frame signals, a frame pulse corresponding to said low-speed frame signal;

switching each of said low-speed frame signals to an appropriate port of said channel according to signals generated from said frame pulses,

wherein the generating includes establishing a frame synchronization on a channel-by-channel basis and outputting said frame pulse which indicates a head position of said low-speed frame signal for each of said received low-speed frame signals, and

the switching includes identifying channel numbers of said low-speed frame signals according to a time difference of said frame pulses, and performing the switching according to said time difference.

12. (Currently Amended) A multiplexing and transmission method used in an apparatus which receives send low-speed frame signals from a plurality of send channels in parallel, outputs a send high-speed serial signal, receives a receive high-speed serial signal, demultiplexes said receive high-speed serial signal into receive low-speed frame signals and outputs said receive low-speed frame signals to a plurality of receive channels in parallel, said multiplexing and transmission method comprising the steps of:

generating control pulses each of which corresponds to one of said send channels, wherein phases of said control pulses are different for each send channel;

receiving said send low-speed frame signal and outputting said send low-speed frame signal in synchronization with said control pulse for each of said send low-speed frame signals; and

multiplexing said send low-speed frame signals into said send high-speed serial signal and outputting said send high-speed serial signal;

demultiplexing said receive high-speed serial signal into said receive low-speed frame signals;

generating, for each of said receive low-speed frame signals, a frame pulse corresponding to said receive low-speed frame signal;

switching each of said receive low-speed frame signals to an appropriate port of said receive channel according to signals generated from said frame pulses,

wherein the generating includes establishing a frame synchronization on a channel-by-channel basis and outputting said frame pulse which indicates a head position of said low-speed frame signal for each of said received low-speed frame signals, and

the switching includes identifying channel numbers of said low-speed frame signals according to a time difference of said frame pulses, and performing the switching according to said time difference.

13. (Original) The multiplexing and transmission method as claimed in claim 10, said multiplexing and transmission method further comprising the step of:

inserting, for each of said low-speed frame signal, a frame synchronization pattern into said low-speed frame signal.

14. (Currently Amended) The multiplexing and transmission method as claimed in claim 10, wherein a time duration on which said control pulses are generated for every channel is smaller than a time duration of a channel-frame format.

15. (Currently Amended) ~~The multiplexing and transmission method as claimed in claim 14, said multiplexing and transmission method further comprising the step of:~~ A multiplexing and transmission method used in an apparatus which receives low-speed frame signals from a plurality of channels in parallel and outputs a high-speed serial signal, said multiplexing and transmission method comprising the steps of:

generating control pulses each of which corresponds to one of said channels, wherein phases of said control pulses are different for each channel;

receiving said low-speed frame signal and outputting said low-speed frame signal in synchronization with said control pulse for each of said low-speed frame signals;

multiplexing said low-speed frame signals into said high-speed serial signal and outputting said high-speed serial signal; and

a selector in said apparatus outputting said control pulses sequentially for each channel according to control clock supplied from a control clock generator, said control pulses generated according to signals supplied from a DC voltage generator;

wherein a time duration on which said control pulses are generated for every channel is smaller than a time duration of a channel-frame format.

16. (Canceled).

17. (Currently Amended) The multiplexing and transmission method as claimed in claim [[16]] 11, said multiplexing and transmission method further comprising the steps of:

shifting each of said frame pulses;

performing an exclusive-OR operation on said frame pulses;

generating a pattern indicating time position of said frame pulse for each of said frame pulses.

18. (Original) A method used in a computer to control a switching circuit in an multiplexing and transmission apparatus which receives a high-speed serial signal and demultiplexes said high-speed serial signal into low-speed frame signals, wherein said

switching circuit assigns each of said low-speed frame signals to an appropriate port of a channel, said method comprising the steps of:

receiving and storing frame pulses indicating head positions of said low-speed frame signals;

checking whether said frame pulses for every channel are stored;

reading said frame pulses and identifying receiving order of said low-speed frame signals; and

controlling said switching circuit on the basis of said receiving order so that said switching circuit assigns each of said low-speed frame signals to an appropriate port of a channel.